REMARKS

By this amendment, Applicants have amended independent claims 11, 13 and 15 to recite that the insulating films are filled in the trenches. See, e.g., Figures 23-31. Independent claims 11, 13 and 15 have been further amended to recite that the dummy regions are formed at a scribing area so as to planarize a surface of the insulating films filled in the trenches at the scribing area by the polishing. See, e.g., paragraph 0152 of Applicants' specification. Dependent claims 12, 14 and 16 have been amended to correct the antecedent basis problem noted by the Examiner. Applicants have also added new independent claim 17 to further define their invention. See, e.g., Figures 23-31 of Applicants' specification.

In view of the foregoing amendments to claims 12, 14 and 16, it is submitted that all of the claims now in the application comply with the requirements of 35 U.S.C. 112, second paragraph. Therefore, reconsideration and withdrawal of the rejection of claims 12, 14 and 16 under 35 U.S.C. 112, second paragraph, are requested.

Claims 11-13, 15 and 16 stand rejected under 35 U.S.C. 102(a) as allegedly being anticipated by U.S. Patent No. 5,614,445 to Hirabayashi. Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hirabayashi. Applicants traverse these rejections and request reconsideration thereof.

Claims 11-17 are directed to a semiconductor integrated circuit device that has at least one trench formed in a semiconductor substrate and a defining active regions and dummy regions. An insulating film is buried in the at least trench by polishing an insulating layer formed over the at least one trench and semiconductor substrate. According to the present invention, the dummy regions are formed at a

scribing area so as to planarize a surface of the insulating film formed in the at least one trench at the scribing area by the polishing.

The patent to Hirabayashi discloses a process for manufacturing a semiconductor device which includes forming trench grooves in an integrated circuit region of a wafer and dummy etched grooves in a scribe line zone of a wafer. Both the trench grooves and the dummy etched grooves are provided with a sidewall insulating film on an inner sidewall and are filled with polycrystalline silicon to provide a smooth wafer surface. The wafer is then cleaved along the scribe line zone. The dummy etched grooves are provided so that the sum of the areas to be etched by dry etching accounts for not less than 5% of the total surface area on one side of the wafer.

In Hirabayashi, the insulating film 8 is formed only on the inner sidewalls of the trench and dummy grooves. The trench and dummy grooves of Hirabayashi are not filled with the insulating film 8. Rather, the trench grooves and dummy grooves of Hirabayashi are filled with polycrystalline silicon. Thus, the Hirabayashi patent does not disclose an insulating film filled in a trench or insulating films filled in a plurality of trenches by polishing an insulating layer formed over the trench(es) and the semiconductor substrate, as presently claimed.

Moreover, the purpose of the dummy etched grooves of Hirabayashi is to make the sum of the areas to be etched not less than 5% of the whole area on one side of the semiconductor wafer so as to suppress side etching. On the other hand, the dummy regions of the present invention are formed at a scribing area so as to planarize a surface of the insulating films filled in the trenches at the scribing by the polishing. Since the purpose of the dummy etched grooves of Hirabayashi is completely different of that of the present invention, it is submitted there would have

been no motivation to modify the teachings of Hirabayashi to arrive at the presently claimed invention.

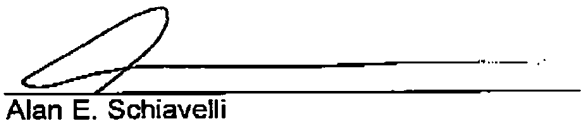
Accordingly, it is submitted that the Hirabayashi patent does not disclose and would not have suggested the presently claimed invention.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.36127CC3), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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